Vertically stacked holey graphene/polyaniline heterostructures with enhanced energy storage for on-chip micro-supercapacitors

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ABSTRACT

Planar micro-supercapacitors (MSCs) have drawn extensive research attention owing to their unique structural design and size compatibility for microelectronic devices. Graphene has been widely used to improve the performance of microscale electrochemical capacitors. However, investigations of an intrinsic electrochemical mechanism for graphene-based microscale devices are still not sufficient. Here, micro-supercapacitors with various typical architectures are fabricated as models to study the graphene effect, and their electrochemical performance is also evaluated. The results show that ionic accessibility and adsorption are greatly improved after the introduction of the holey graphene intermediate layer. This study provides a new route to understand intrinsic electrochemical behaviors and possesses exciting potential for highly efficient on-chip micro-energy storage.

1 Introduction

The rapid development of electronic techniques, which has added great convenience to people's lives in past decades, is moving toward miniaturization and multifunctionality [1, 2]. On-chip energy storage devices will play key roles in future microelectronics [3–5]. From the perspective of practical use, on-chip electrochemical energy storage units (OEESUs), typically microbatteries and micro-supercapacitors (MSCs), possess highly desired characteristics such as large energy/power densities, high rate capability, and long

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lifespan [6–8]. Recently, OEESUs with interdigital electrodes have been achieved using microelectro-mechanical systems fabrication techniques and are considered as favorable choices for efficient on-chip energy storage [9].

MSCs often offer much higher power delivery compared with microbatteries by storing the charges in few minutes or even seconds [10]. Electrical double-layer micro-supercapacitors (EDL-MSCs) were first developed as typical MSCs, which mainly rely on ionic absorption and deabsorption. The Müllen group recently reported on graphene-based in-plane inter-digital MSCs with a thickness of ~15 nm that allow for operations at ultrahigh rates up to 1,000 V·s^{-1} [11]. Compared with EDL-MSCs, electronically conducting polymer (ECP)-based micro-pseudocapacitors store charges through doping and dedoping, which are faradic redox reactions, along with ionic absorption and deabsorption [12]. In general, their energy densities are higher than those of electrical double layer capacitors (EDLCs). Polyaniline (PANI), a unique material among ECPs, has aroused broad concern owing to its high theoretical pseudocapacitance, good environmental stability, and simple acid-based faradic charge transfer processes [13–16]. It is well known that graphene can improve the electrical conductivity of pseudocapacitive ECP-based electrodes [17–22]. However, in theory, the layered structure of graphene limits the ion transportation between neighboring layers of graphene during the charge/discharge pro-cesses. Thus, the function of graphene in MSC, and how graphene influences the intrinsic electrochemical behaviors, need to be further investigated.

Here, to study the intrinsic electrochemical behaviors of planar MSCs, we designed and fabricated MSCs with various typical architectures as models to understand the graphene effect. Graphene and holey graphene (h-Graphene) intermediate layers are intro-duced between thin PANI film and current collectors. Compared with an unmodified graphene intermediate layer, the h-Graphene intermediate layer not only enhances the electrical conductivity between PANI and gold but also enables electrolyte ions to get across the neighboring h-Graphene planes and ultimately gain access to inner PANI surfaces. Electrochemical per-formance tests show that the ultrahigh stack capacitance and energy density of OEESUs with vertically stacked h-Graphene/polyaniline heterostructures (h-GPHs) reach 271.1 F·cm^{-3} and 24.1 mW·h·cm^{-3}, respectively, which are much higher than those of MSCs with bare-PANI-based interdigital structures (PISs) and vertically stacked unmodified graphene/polyaniline heterostructures (u-GPHs). The rate capability of OEESUs with h-GPHs is also largely enhanced. Their ultrahigh energy and power density deliveries demon-strate that our strategy provides new insights for understanding the intrinsic electrochemical processes and designing high-performance on-chip micro-energy storage devices.

2   Experimental

2.1   Synthesis of h-Graphene oxides

To fabricate holey graphene sheets, GO suspension was first synthesized by a modified Hummers' method and diluted to ~0.1% w/w by deionized water [23, 24]. Then, the diluted GO suspension was mixed with 70% concentrated HNO$_3$ (1:10 in volume ratio) by stirring, followed by sonication at room temperature for 1 h. After sonication, the mixture was settled for 1 h at room temperature and then washed with deionized water to obtain the resulting holey GO suspension [25].

2.2   Fabrication of h-GPH-based MSCs

A silicon substrate with 300-nm-thick SiO$_2$ was washed with an isopropyl alcohol solution and used as the substrate. The photoresist 9000A was spin-coated and baked on the substrate. After that, lithography and physical vapor deposition techniques were used to fabricate the interdigital patterns and Ti/Au (3/17 nm) layer. Then, the h-Graphene oxide intermediate layer was deposited on the current collectors by the drop-dry technique and was reduced by the diluted hydrazine hydrate solution. The PANI layer (~20 nm) was then electropolymerized on the h-Graphene intermediate layer (~20 nm) through the cyclic voltammetry (CV) method at a scan rate of 30 mV·s^{-1} for five cycles ranging from −0.2 to 1.6 V in a three-compartment system where interdigital electrodes, Hg/HgO, and Pt foil were used as the working electrode, reference electrode, and counter electrode, respectively. This electropolymerization

was performed in the electrolyte of 1 mL of aniline and 200 mL of 0.01 M H_2SO_4. After electropolymerization, the chip was carefully washed in dilute acid to remove most of the unreacted aniline monomer. Then, the 1 M H_2SO_4 was dropped onto the interdigital electrodes and used as the electrolyte of the on-chip energy storage devices. Polyvinyl alcohol-H_2SO_4 gel electrolyte was prepared by dissolving 6 g of polyvinyl alcohol in 60 mL of 1 M H_2SO_4 solution. All experiments were carried out at room temperature.

2.3 Characterization of interdigital electrodes and devices

The heights of on-chip MSCs with PISs, u-GPHs, and h-GPHs were measured by a stylus surface profiler (Bruker DektakTX), and the morphology was observed by a field-emission scanning electron microscope (FESEM) (JEOL JSM-7100F) with an acceleration voltage of 20 kV. The transmission electron microscopic (TEM) images were obtained using a JEOL JEM-2100F microscope. XPS analysis was performed by VG Multilab 2000, and Raman spectra were collected by a Renishaw RM-1000 laser Raman microscopy system. CV curves, galvanostatic charge–discharge curves, and electrochemical impedance spectra were recorded using an Autolab PGSTAT302N. All measurements were performed at room temperature.

3 Results and discussion

The fabrication process for on-chip MSCs with h-GPHs is illustrated in Fig. 1. The SiO_2/Si substrate was employed as the substrate, and the as-deposited patterned Ti/Au (3/17 nm) layer acted as the current collector. After obtaining the graphene oxide (GO) solution by a modified Hummers' method, the in-plane pores were formed by combining ultrasonic vibration with mild acid oxidation processes [25]. The h-Graphene oxide layers were formed after repeating drop-dry processes several times, and the thickness was carefully controlled by the concentration of GO solution and the drying rate. Then, h-Graphene oxide layers were reduced to h-Graphene by diluting the hydrazine hydrate solution. Thereafter, a three-electrode system was applied to directly grow the PANI layer using the CV sweep method. During the electropolymerization process, the symmetrical interdigital electrodes, including the cathode and anode electrodes of the MSCs, both acted as the working electrodes. After electropolymerization, h-GPHs were achieved, and 1 M H_2SO_4 solution was utilized as the electrolyte for electrochemical measurements. For a fair comparison, the on-chip MSCs with u-GPHs and PISs were also carried out on the same interdigital Ti/Au current collectors.

The digital camera image of the OEESUs, as shown on the left of Fig. 2(a), reflects the appearance of as-
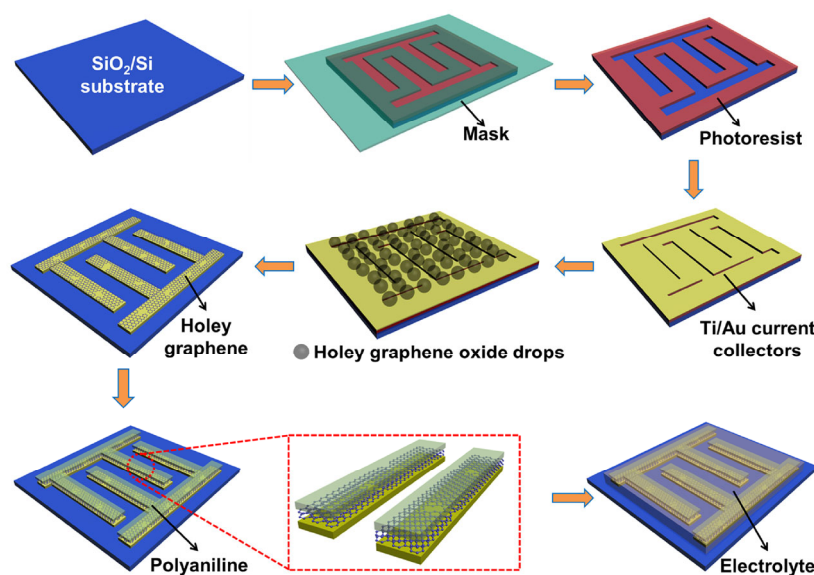

Figure 1 Schematic illustration of fabrication process for on-chip MSCs with h-GPHs.

prepared tiny on-chip MSCs whose size is comparable to commercialized microelectronic devices. The width of each interdigital finger is ~150 μm, and the interspace is ~50 μm (Fig. 2(a), right), indicating the high areal utilization of active materials (75%). It is confirmed from Figs. 2(b) and 2(c) that the as-deposited materials are well covered on the patterned Ti/Au current collectors and that the photoresist between each of the two electrodes is mostly removed. After hydrazine hydrate treatments, it is found that the surface of the h-Graphene intermediate layer becomes crumpled (Figs. 2(d) and 2(e)), which indicates more in-plane space of the graphene intermediate layer. To take a deeper look at h-GPHs, a TEM measurement was taken (Fig. 2(f) and Fig. S1 in the Electronic Supplementary Material (ESM)), showing that both PANI and h-Graphene intermediate layers exhibit ultrathin morphology and that the porosity can also be found,

which is consistent with previous Ref. [25].

The Raman spectrum of pure PANI film (λ = 633 nm) is shown in Fig. S2(a) in the ESM, and the characteristic peaks can be easily observed. The 1,171 cm⁻¹ band corresponds to the benzene C–H bending deformation, and the 1,249 cm⁻¹ band corresponds to the C–N stretching. The strong peak centered at 1,370 cm⁻¹ can be assigned to C–N•⁺ stretching. The positions of C=N stretching and N–H bending deformation fall at 1,470 and 1,514 cm⁻¹, respectively. The peak at 1,589 cm⁻¹ is attributed to the C–C benzene deformation [26]. Fourier transformed infrared (FTIR) spectroscopy was further utilized to characterize the PANI film, as shown in Fig. S2(b) in the ESM. The 1,487- and 1,578-cm⁻¹ peaks both correspond to the C=C stretching vibrations of the benzenoid ring and quinoid (Q) ring. The peaks centered at 1,130 and 1,306 cm⁻¹ are attributed to the
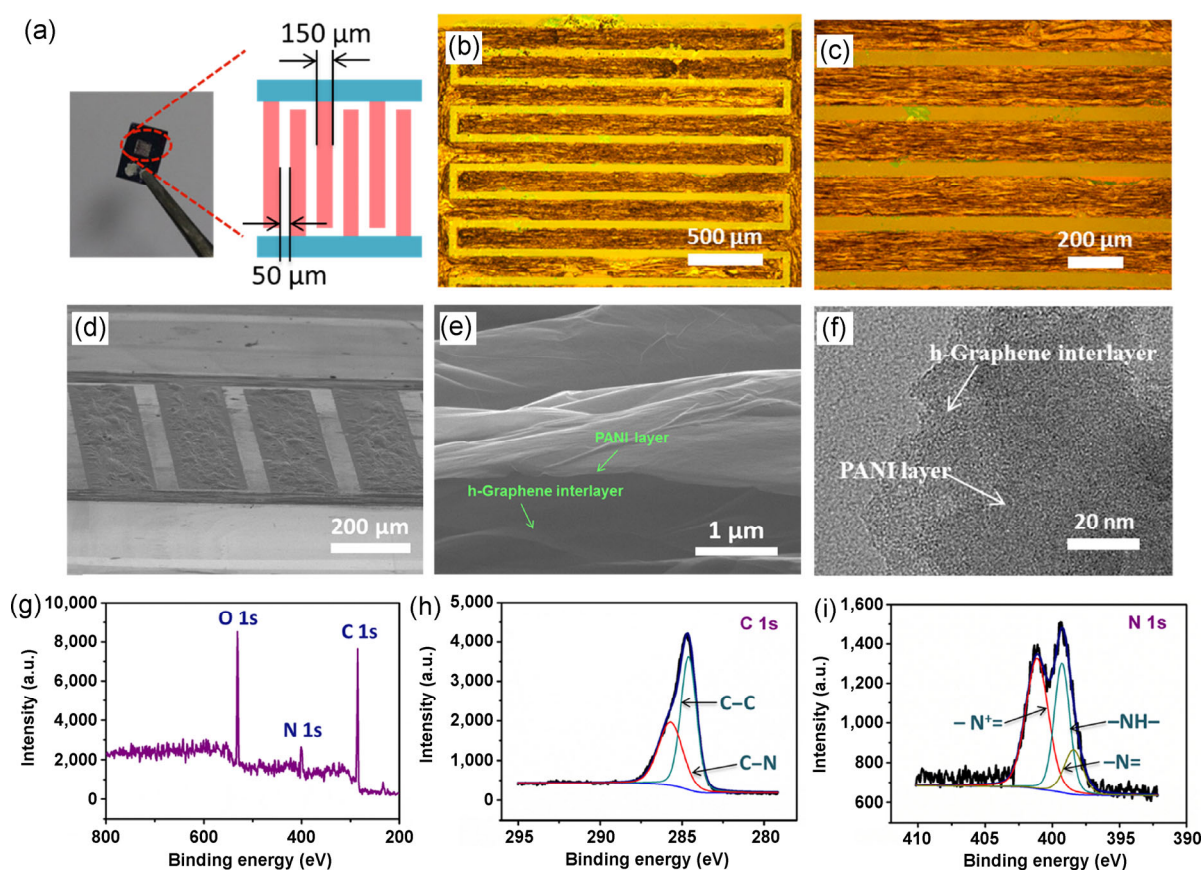

Figure 2 Configuration of h-GPH-based on-chip MSCs. (a) Digital camera image of MSCs (left) and schematic illustration of interdigital electrodes (right). (b) and (c) Bright-field optical images of MSCs. (d) and (e) FESEM images of MSCs viewed at tilted angles. (f) TEM image of PANI/h-Graphene hybrid structure. (g) XPS spectra and high-resolution XPS spectra of (h) C 1s and (i) N 1s of h-GPH-based MSCs.

N=Q=N stretching band and C–N stretching mode, respectively. The peak at 3,400 cm^{-1} can be assigned to the stretching vibration N–H of aromatic amine along with the stretching vibration of absorbed water. These results are consistent with our previous work and confirm the existence of PANI films [27].

To further characterize the chemical components and valence states of the h-GPH-based micro-electrodes, X-ray photoelectron spectroscopy (XPS) analysis was utilized in this experiment (Fig. 2(g)). The three elemental signals, namely C 1s, N 1s, and O 1s peaks, are observed in the XPS spectra of h-GPHs. The peak of C 1s, centered at approximately 284.6 eV, is mainly ascribed to the C–C bonds at 284.7 eV and C–N bonds at 285.7 eV (Fig. 2(h)), which demonstrates the existence of an h-Graphene intermediate layer and the carbon atoms' contact with the surface of the as-deposited PANI layer, respectively. Figure 2(i) reveals the presence of the PANI layer and the valence states of nitrogenous groups. Three important bonds—benzenoid amine (–NH–) at 399.0 eV, quinonoid imine (–N=) at 398.2 eV, and a nitrogen cationic radical (–N^{+}=) at 400.5 eV—contribute the N 1s spectrum, which shows the states between the h-Graphene intermediate layer and the PANI layer [28, 29]. Raman spectroscopy of the on-chip MSCs was carried out to further investigate the introduction of h-Graphene in the hybrid architecture (Fig. S3 in the ESM). After the deposition of graphene and h-Graphene intermediate layers, the emergence of peaks of the D band and G band located at approximately 1,323 and 1,591 cm^{-1}, respectively, are clearly manifested in the Raman spectrum. The D-band and G-band intensity ratios (denoted as the I_{D}/I_{G} ratio) were calculated to examine their difference in sp^{3} and sp^{2} contents, which were measured at 1.137 and 1.723 for graphene and h-Graphene, respectively. The higher I_{D}/I_{G} ratio value suggests more defects of h-Graphene sheets in the interdigital heterostructures, which further confirm the holes' existence and structural information of the h-Graphene intermediate layer [30, 31]. The degree of oxidation of h-Graphene oxides can be clearly identified from the C 1s XPS spectrum (Fig. S4(a) in the ESM). Four functional groups, namely non-oxygenated ring C–C bonds, C–O bonds, C=O bonds, and O–C=O bands, correspond to

the four different peaks centered at 284.5, 286.4, 287.8, and 288.9 eV, respectively. After the reduction treatment, the sharp decrease of the C–O bonds' peak, C=O bonds, and O–C=O bands (Fig. S4(b) in the ESM) indicates a high reduction degree of the h-Graphene oxide intermediate layers.

The electrochemical behaviors of the fabricated devices were tested in symmetrical two-electrode systems. CV curves were measured at various scan rates from 20 to 10,000 mV·s^{-1}. A typical asymmetrical potential window ranging from 0 to 0.8 V was selected along with the comparison of PISs, u-GPHs, and h-GPHs. At the low scan rate of 20 mV·s^{-1}, a pair of small redox peaks in the CV curves was observed, which indicates the occurrence of a redox reaction (Fig. 3(a)) [32], while for graphene the nearly rectangular shape shown in Fig. S5 indicates ideal double-layer supercapacitor behaviors. The redox peaks shifted to the left after the h-Graphene intermediate layer was introduced (Fig. 3(b)). Obviously, as evidenced by Fig. 3(c), the altitudes of the peak current for h-GPHs are much enlarged compared with those of bare PISs and u-GPHs, representing the greatly increased accessibility of electrolyte ions.

Based on the CV curves, we calculated the stack capacitance (C_{s}, in F·cm^{-3}), energy density (E, in W·h·cm^{-3}), and different average power density (P_{av}, in W·cm^{-3}) to understand the intrinsic properties of the nanostructure designs [4, 33]. These values are calculated using the following equations

$$C_{s} = \frac{\int I \mathrm{d}V}{v(\Delta V)S} \tag{1}$$

$$E = \frac{C_{s}(\Delta V)^{2}}{7,200} \tag{2}$$

$$P_{av} = \frac{E}{\Delta t} \times 3,600 \tag{3}$$

where I is the current (in A); v is the scan rate (in V·s^{-1}); ΔV is the operation potential window (in V); S is the total volume (in cm^{-3}) of the device including cathode, anode, current collectors, and electrolyte; and Δt is the discharge time. The stack capacitance of the MSC based on bare PISs is 17.4 F·cm^{-3} at a scan
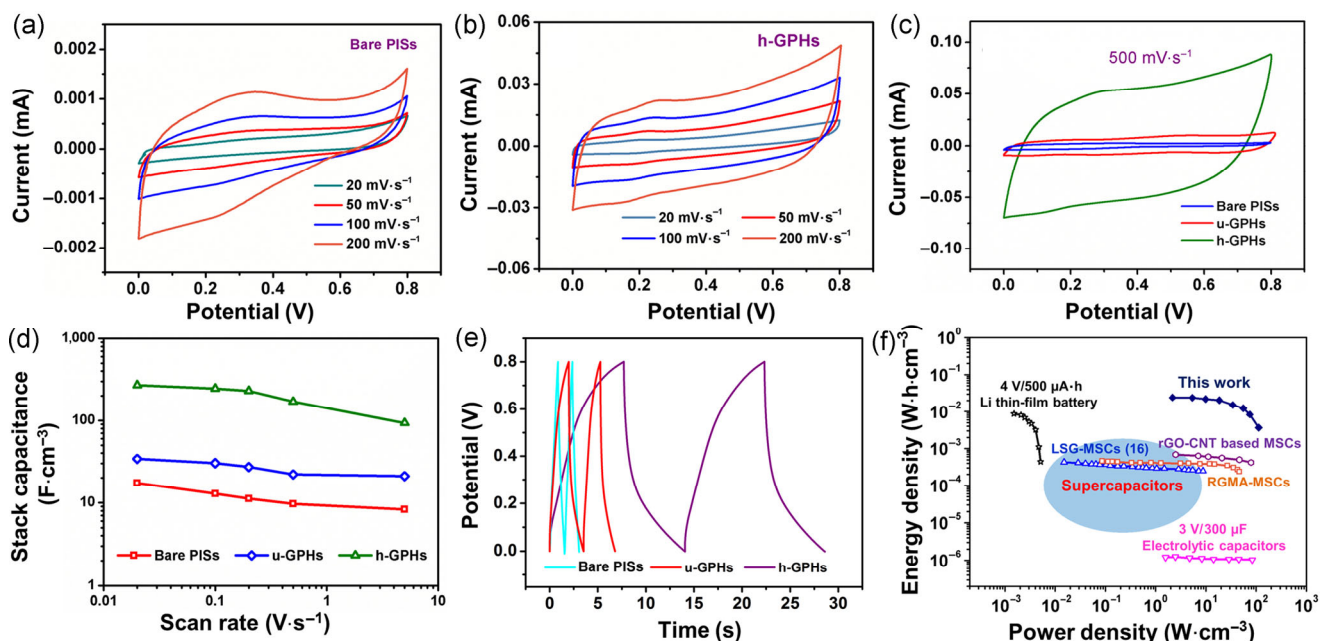
Figure 3 Electrochemical performance of on-chip MSCs. (a)–(c) CV curves of MSCs at various scan rates in 1 M H$_2$SO$_4$ in potential window from 0 to 0.8 V. (d) Stack capacitance evolution of MSCs at different scan rates in potential window from 0 to 0.8 V. (e) Galvanostatic charge–discharge curves of MSCs with bare PISs, u-GPHs, and h-GPHs from 0 to 0.8 V at current density of 100 μA·cm^{-2}. (f) Ragone plot of volumetric energy density versus power density for h-GPH-based MSCs in comparison with typical batteries, electrolytic capacitors, supercapacitors, LSG-MSCs, RGMA-MSCs, and rGO-CNT-based MSCs.

rate of 20 mV·s^{-1}, which is superior to the volumetric capacitance of some recently reported EDL-MSCs [34, 35]. After introducing the ultrathin graphene intermediate layer (~20 nm), the stack capacitance increased to 34.1 F·cm^{-3}, which is attributed to the enhanced electrical transport of PANI and additional in-plane ionic absorption of graphene (Fig. S6 in the ESM). A remarkable specific capacitance and energy density (up to 271.1 F·cm^{-3} and 24.1 mW·h·cm^{-3}, respectively) are achieved for h-GPH-based MSCs, indicating high ionic accessibility during the charge and discharge processes. At a scan rate of 500 mV·s^{-1}, the h-GPH-based MSCs exhibit a high stack capacitance of 170.3 F·cm^{-3} (Fig. 3(d)). As shown in Fig. S7 (see ESM), the specific stack capacitance of h-GPH-based MSCs is still up to 27.5 F·cm^{-3} at an ultrahigh scan rate of 10,000 mV·s^{-1}. Moreover, according to Eq. (3), the stack power density reaches 110.1 W·cm^{-3}, indicating the high rate capability of h-GPH-based MSCs. The cycling performance at a scan rate of 5,000 mV·s^{-1} for the MSCs with h-GPHs is shown in Fig. S8 in the ESM. It can be clearly seen that this heterostructure exhibits

excellent reversible capacitance (99.5% capacitance retention) over 5,000 charge–discharge cycles.

The stack capacitance C_s is also calculated from the galvanostatic charge–discharge curves (Fig. 3(e)) according to the following equation

$$C_s = \frac{I\Delta t}{S\Delta V} \tag{4}$$

where I is the discharge current (in A), Δt is the discharge time (in s), S is the total volume of the device (in cm^{-3}), and ΔV is the potential window (in V) excluding the IR drop. The stack capacitance value is calculated to 158.9 F·cm^{-3} for h-GPH-based MSCs at a current density of 100 μA·cm^{-2}, which is much higher than those of PISs and u-GPH-based MSCs. This further indicates the significant advantages of h-GPH micro-electrodes.

Based on the data of energy density and power density of MSCs with h-GPHs, a Ragone plot is provided in Fig. 3(f). It can be clearly seen that the electrochemical performance of h-GPH-based MSCs is superior to those of laser-scribed graphene MSCs

(LSG-MSCs) [36], reduced graphene oxide/manganese dioxide/Ag nanowire MSCs (RGMA-MSCs) [13], and rGO-CNT-based MSCs [37]. This demonstrates the significant advantages of h-GPH-based on-chip MSCs with largely enhanced ion accessibility compared with previous reports. In addition, solid-state MSCs with h-GPHs were also successfully fabricated and tested using polyvinyl alcohol-H_2SO_4 gel electrolyte, as shown in Fig. S9 in the ESM. At a scan rate of 500 mV·s^{-1}, the stack capacitance of h-GPH-based MSCs in liquid electrolyte is 170.3 F·cm^{-3}, and the solid-state h-GPH-based MSCs still deliver a high stack capacitance up to 102.0 F·cm^{-3}, which is very promising for practical use compared with most previous reports.

During the charge–discharge processes, ion migration in the electrolyte takes place between each of the two fingers in interdigital structures to realize the output of energy (Figs. 4(a) and 4(b)). However, for various electrode architectures, their charge storage mechanisms have essential differences, which are schematically illustrated in Fig. 4(c). (I): For bare PISs, only the electrode surface and side parts are exposed to the electrolyte. Thus the ion absorption and redox reaction are only accessible to these active surface areas, indicating low capacitance of the PANI for energy storage. (II): In contrast to bare PISs, u-GPHs allow faster electron diffusion between the PANI and gold. Furthermore, the electrolyte ions can also be absorbed in the graphene in-plane space, indicating an increased specific capacitance of OEESUs. The existence of interfacial contact between graphene and PANI could also ensure robust binding with the current collectors. However, as evidenced by the electrochemical performance, this ion migration takes place only between the graphene planes, and most of the PANI bulk are still inaccessible for these ions. (III): Compared with the unmodified graphene intermediate layer, the in-plane pores of the h-Graphene intermediate layer ensure ion transfer from h-Graphene ultimately to the inner PANI layer, which reveals the abundant ion accessibility in this charge storage mechanism. It is believed that the number of ions that get access from h-Graphene is much higher than that of ions absorbed on the surface of bare PANI electrodes because of easier electron
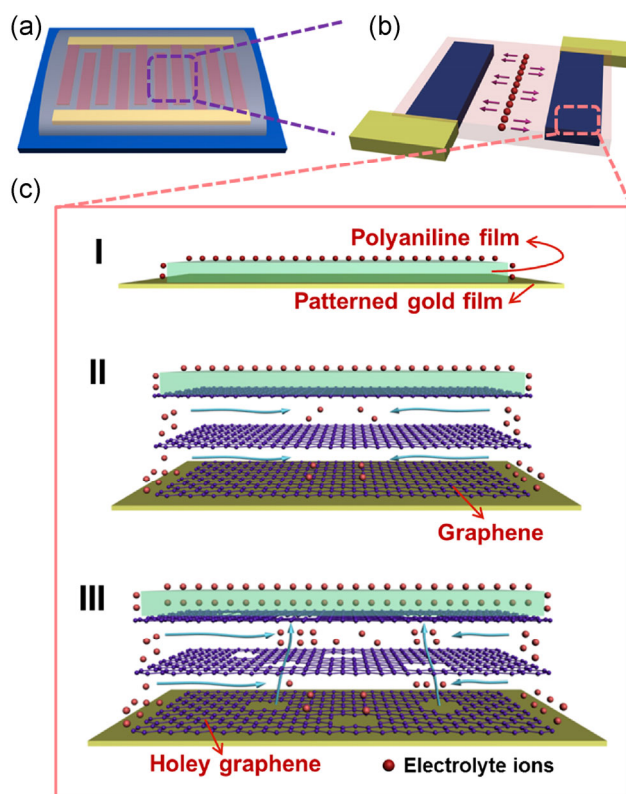

Figure 4 Different charge storage mechanisms of interdigital-electrode-based on-chip MSCs. (a) Schematic illustration of planar structure. (b) Simple description of charging and discharging processes in two symmetrical micro-electrodes. (c) Three different ion transport modes in (I) bare PISs, (II) u-GPHs, and (III) h-GPHs.

access. Furthermore, considering the redox capacitive contribution and interior electrical transport, the electrochemical performance of MSCs would also be largely influenced by the thickness of the PANI film.

The enhanced ionic accessibility and diffusion of h-GPH-based MSCs compared with those of u-GPHs and bare PIS-based MSCs are further supported by AC impedance spectra, as shown in Fig. S10 in the ESM. In the bode plot (Fig. S11 in the ESM), a −45° phase angle was present at 398 Hz for h-GPH-based MSCs, at 175 Hz for u-GPH-based MSCs, and at 172 Hz for bare-PIS-based MSCs. Thus the corresponding time constant is 2.5 ms, which is much shorter than that of bare PISs and u-GPH-based MSCs. This strongly suggests the greater advantages of instantaneous high power and energy delivery. This novel charge storage mechanism results in greatly improved volumetric energy densities that are comparable or even superior

to microbatteries. Meanwhile, it is widely acknowledged that the maximum power density (P_{max}) is a key property for OEESUs. Based on the equivalent series resistance (ESR) value, the maximum power density of h-GPH-based MSCs is calculated by $P_{max} = V_i^2/(4 \times ESR \times S)$, where V_i represents the initial voltage in the charge–discharge processes, and S is the total volume of the device [38–41]. The maximum power density of h-GPH-based MSCs is over 1,000 W·cm^{-3}, which approaches the power density of electrolytic capacitors. The h-GPHs demonstrate a highly efficient on-chip energy storage strategy, as evidenced by their excellent electrochemical properties.

4 Conclusions

In summary, the essential function of graphene in MSCs and how graphene influences their intrinsic electrochemical behaviors are investigated. By introducing the h-Graphene intermediate layer, electrolyte ions can get access to the h-Graphene in-plane space and inner PANI layer. Thus more electrolyte ions are absorbed and more drastic redox reactions occur during the charge–discharge process. The on-chip MSCs with h-GPHs exhibit much higher stack capacitance and energy density compared with those of bare-PIS-based MSCs. Furthermore, the unique heterostructure-architecture-based MSCs exhibit high rate capability and outstanding cycling stability. This study provides a new route to understand intrinsic electrochemical behaviors, which are crucial for fabricating next-generation on-chip energy storage devices with ultrahigh energy and power densities. The novel strategy possesses broad application prospects in the microelectronic and electrochemical industries.

Electronic Supplementary Material: Supplementary material (TEM images, Raman spectrum, XPS spectra, CV curves, cycling performance, AC impedance spectra, and Bode plot) is available in the online version of this article at http://dx.doi.org/10.1007/s12274-016-0989-x.

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